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Ferroelectric topologically configurable multilevel logic unit

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Abstract

Multilevel devices demonstrating switchable polarization enable us to efficiently realize neuromorphic functionalities including synaptic plasticity and neuronal activity. Here we propose using the ferroelectric logic unit comprising multiple nanodots disposed between two electrodes and coated by the dielectric material. We devise the integration of the ferroelectric logic unit, providing topologically configurable non-binary logic into a gate stack of the field-effect transistor as an analog-like device with resistive states. By controlling the charge of the gate, we demonstrate the various routes of the topological switchings between different polarization configurations in ferroelectric nanodots. Switching routes between different logic levels are characterized by hysteresis loops with multiple branches realizing specific interconnectivity regimes. The switching between different types of hysteresis loops is achieved by the variation of external fields and temperature. The devised ferroelectric multilevel devices provide a pathway toward the novel topologically-controlled implementation of discrete synaptic states in neuromorphic computing.

1. Introduction

Existing computing circuits employ the standard binary logic for storage and processing information. However, these circuits have reached their fundamental limitations set by the atomic size miniaturization and by the fundamental Landauer principle of energy dissipation per bit processing [1]. Utilizing many-valued logic units reduces energy losses and enables combining the memory and computational units within a single chip, processing unprecedentedly high-density information and overcoming thus the binary tyranny [2, 3]. Exploring the multilevel non-binary logic crucial for realizing non-von Neumann computing is an unresolved daunting task calling for a breakthrough in the search for systems capable to carry switchable logic multistate medium [4, 5].

The emergence of a new paradigm of neuromorphic computing emulating the process of the human brain, using precise electrical currents to flow between the synapse of the neurons, stimulates the search for new materials that can fulfill the functionality of synaptic plasticity and neuronal activity [6–8]. At the same time, the existing artificial neural networks are implemented via the energy-consuming binary circuits comprising the in-series connected central processing and binary memory units [9, 10]. The implication of the neuromorphic computing architecture having multilevel synaptic weights will incredibly increase the performance, overcoming the barriers of the von Neumann computing circuits [11, 12].

However, existing implementations of the multilevel logic unit that are currently used in the solid-state drives and flash memories require the analog methods of the bits writing [13], leading to the erratic behavior of the logic cells due to stochastic loss of information. In this consideration, ferroelectric materials are the promising candidates offered the unique properties of implementation multiple polarization states, which make them the prime platform for utilizing them as more energy-efficient elemental units for the multilevel devices capable of exercising a non-binary logic [8, 14–16]. Moreover, multi-valued logic has particular importance in light of the development of multilevel neuromorphic architecture, complementary to field-effect transistor technology [17].

In this paper, we propose an implementation of the charge-driven multilevel logic unit on the base of the ferroelectric materials that keep the spontaneously ordered dipolar charges resulting in spontaneous electric polarization. The suggested multilevel logic unit comprises several ferroelectric nanodots disposed between two electrodes and coated by the dielectric material of the distinct nanodots. Switching between different polarization configurations of the nanodots and realizing the different multilevel states is achieved by putting the charge on the electrodes, similar to what happens in the synaptic computing of the brain-inspired logic. We suggest novel technology for non-invasive control of the memory-level access architecture by modification of the topology of the hysteretic switching sequence via external stimuli, temperature, and strain. On the device-architecture level, the suggested ferroelectric unit with a charged-driven multilevel logic and topologically-controlled access to the logic states realizes the artificial neuron with multilevel synaptic weights. It can be implemented as a gate stack containing several ferroelectric nanodots and incorporated into the field-effect transistor. The topological switching between different states is achieved by the specific protocol of the operating spike pulses of the external voltage.

2. Binary logic unit

We first describe the building block of the multilevel-logic unit, a single ferroelectric nanodot confined between two electrodes. Figures 1(a) and (b) show the ferroelectric nanodots with different orientations of polarization. Every ferroelectric nanodot is uniformly polarized and is confined between the two conducting electrodes carrying the electric charge. It can stay in either of two ferroelectric states, the state $(+)$, having the polarization directed 'up' and the state $(-)$ having the polarization directed 'down,' implementing, thus, two corresponding logical levels, $|+1\rangle$ and $|-1\rangle$. The polarization of ferroelectric P in the electric field E is described by the constitutive relation $P = \pm P_s + \varepsilon_0\varepsilon_f E$ where signs $\pm$ correspond to the 'up' or 'down' orientation of spontaneous polarization P_s, ε_0 is the vacuum dielectric permittivity, and ε_f is the dielectric constant of the ferroelectric material. This constitutive relation provides the two-branch ferroelectric hysteresis loop $P_\pm(E)$, see figure 1(c). The transition from the state $(-)$ to the state $(+)$ occurs at the coercive field E_c and transition from the state $(+)$ to the state $(-)$ at the coercive field $-E_c$.
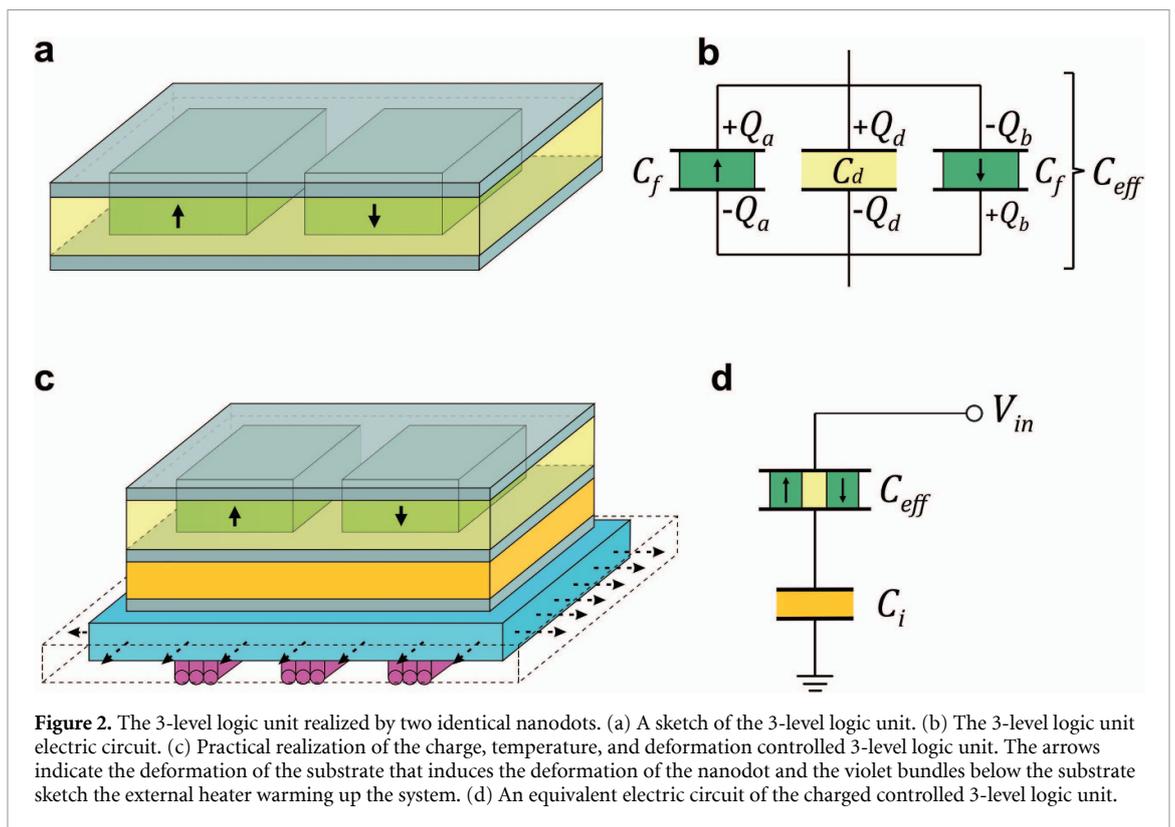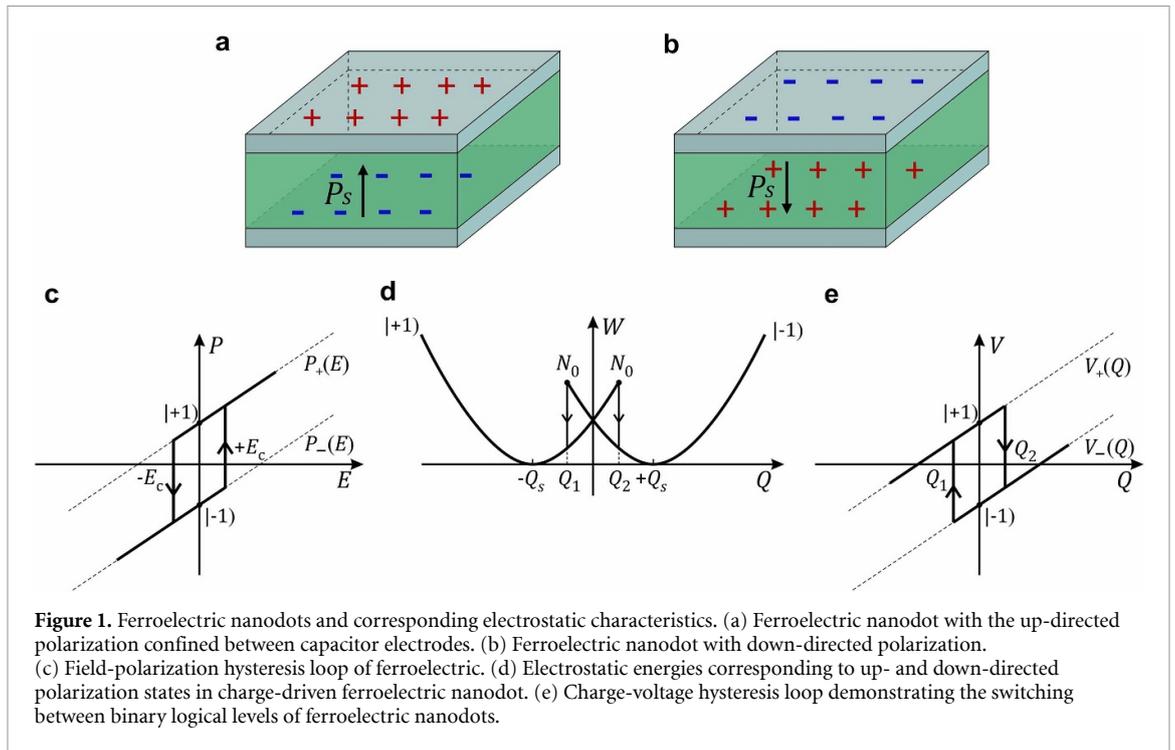
In general, the orientation of the polarization in the nanodot is controlled by the electric state of the conducting electrodes that can be operated either by the applied voltage or by the applied charge. Here we consider the latter functioning mode, which we call the charge operation regime. In this regime, the charge, Q, imposed on the conducting electrodes creates the electric field, which interacts with the polarization field of the nanodot.

A single ferroelectric nanodot confined between the capacitor's electrodes implements a two-level binary logic unit. Importantly, the effective electric field, E, operating the polarization of the nanodot includes not only the field induced by the charge Q at the conducting electrodes but also by the depolarization field, E_d, induced by the bound charge, $Q_s = SP_s$, emerging at the polarization field lines termination points located at the interface between the ferroelectric nanodot and the conducting electrode. Hence, the voltage, V, at the single ferroelectric nanodot capacitor is given by $C_f V = Q \pm Q_s$, where $C_f = \varepsilon_0\varepsilon_f S/d$ is the capacitance of the ferroelectric material.

Figure 1(c) exemplifies the behavior of electrostatic energies, $W_\pm = (Q \pm Q_s)^2/2C_f$ corresponding to the $(+)$ and $(-)$ polarization states, respectively, with the spontaneous polarization $\pm P_s$ as functions of the applied charge Q. The branches $W_\pm$ are shifted over $\pm Q_s$ over the Q-axes with respect to $Q = 0$, and the minima correspond to situations where the conducting electrode charge precisely compensates the bound charge, which results in the zero internal field. The terminal points, N_0, of parabolas correspond to the situation where a state with the given polarization direction becomes unstable with respect to switching to the state with the opposite polarization direction. The critical charges corresponding to the switching instabilities $(-) \rightarrow (+)$ and $(+) \rightarrow (-)$ are given by $Q_{1,2} = \pm(Q_s - Q_c)$ respectively, where $Q_c = C_f E_c d$. The energy profile $W_\pm(Q)$ results in the charge-voltage two-branch switching hysteresis loop $V(Q)$ with upper and lower branches $V_\pm(Q) = C_f^{-1}(Q \pm Q_s)$ corresponding to the logical levels $|+1\rangle$ and $|-1\rangle$, respectively, as shown in figure 1(d).

3. The 3-level logic unit

A 3-level logic unit comprises two identical binary units electrically communicating through the common electrodes. An exemplary device realizing the 3-level logic unit is shown in figure 2(a). Two identical, for example, rectangular ferroelectric nanodots, with equal coercive fields, E_c, and equal cross-sections, S_f, are confined between the conducting electrodes and embedded into the dielectric material with dielectric constant ε_d, filling up the residual space between conducting electrodes. As a whole, the construction realizes a capacitor with the plane area S and thickness d. The system is driven by applying the electrical charge, Q,

Figure 1. Ferroelectric nanodots and corresponding electrostatic characteristics. (a) Ferroelectric nanodot with the up-directed polarization confined between capacitor electrodes. (b) Ferroelectric nanodot with down-directed polarization. (c) Field-polarization hysteresis loop of ferroelectric. (d) Electrostatic energies corresponding to up- and down-directed polarization states in charge-driven ferroelectric nanodot. (e) Charge-voltage hysteresis loop demonstrating the switching between binary logical levels of ferroelectric nanodots.

Figure 2. The 3-level logic unit realized by two identical nanodots. (a) A sketch of the 3-level logic unit. (b) The 3-level logic unit electric circuit. (c) Practical realization of the charge, temperature, and deformation controlled 3-level logic unit. The arrows indicate the deformation of the substrate that induces the deformation of the nanodot and the violet bundles below the substrate sketch the external heater warming up the system. (d) An equivalent electric circuit of the charged controlled 3-level logic unit.

onto conducting electrodes, providing the set of polarization states, 'up-up' $(++)$, 'up-down' $(+-)$ (shown in figure 2(a)), and 'down-down' $(--)$ (note that the state $(-+)$ is equivalent to the state $(+-)$), realizing, thus, the 3-level logic, characterized by the logic levels $|+1\rangle$, $|+0\rangle$ and $|-1\rangle$, respectively. Importantly, the driving charge Q can be distributed nonuniformly over the conducting electrode, forming the charge Q_a in the region of the first nanodot, the charge Q_b in the region of the second nanodot, and the charge Q_d in the region of the dielectric spacer. An effective electric circuit of the system is shown in figure 2(b). It includes two equivalent ferroelectric capacitors C_f and one dielectric capacitor C_d connected in parallel. The charges Q_a, Q_b, and Q_d of the corresponding capacitors are defined by the equality of the potential at the electrodes

of the capacitors and are determined by the condition $C_f^{-1}(Q_a \pm Q_s) = C_f^{-1}(Q_b \pm Q_s) = C_d^{-1}Q_d$, taking into account that $Q_a + Q_b + Q_d = Q$. Here every particular combination of pluses and minuses corresponds to the given polarization state of the system, $C_f = \varepsilon_0\varepsilon_f S_f/d$ is the capacitance of the ferroelectric material, and $C_d = \varepsilon_0\varepsilon_d(S - 2S_f)/d$ is the capacitance of the dielectric spacer. From the above condition, one obtains $Q_{a,b} = (C_f/C_{eff})Q \pm Q_s$, $Q_d = (C_d/C_{eff})Q$, where $C_{eff}^{-1} = 2C_f^{-1} + C_d^{-1}$ is the effective capacitance of the entire system.

Figure 2(c) presents the realization of the charge, temperature, and deformation control of the polarization states in the exemplary device with the 3-level logic. The equivalent electric circuit demonstrating the charge control of the exemplary device with the 3-level logic is presented in figure 2(d). The additional capacitor, with the capacitance C_i containing the dielectric spacer integrated into the full system, is disposed below the exemplary device with the 3-level logic, sharing with it the common conducting electrode. The whole system, therefore, comprises two capacitors (the exemplary device with the 3-level logic and the additional capacitor connected in series), as shown in figure 2(d). The top conducting electrode and the bottom conducting electrode of the additional capacitor play the role of the electrodes to which the incoming voltage V_{in} is applied. The charge at the conducting electrodes of the exemplary device with the 3-level logic induced by the voltage V_{in} and is given by the equation $V_{in} = Q/C_i + V(Q)$ where $V(Q)$ is the voltage determined by the charge-voltage characteristics of the exemplary device with the 3-level logic described below. This relation becomes particularly simple and transforms to $Q \approx C_i V_{in}$ when the effective capacitance of the exemplary device with the 3-level logic substantially exceeds the capacitance of the additional capacitor. The charge that controls the polarization state of the exemplary device with the 3-level logic is directly tuned by the voltage V_{in} applied to the whole system. Being heated by the built-in heater, the substrate changes the temperature of the device. For example, the applied temperature is about room temperature, and the temperature variation ΔT can be of the range 10–300 K. Also, the heating and cooling of the substrate lead to its mechanical deformation that generates the strains in the exemplary device with the 3-level logic. Alternatively, the strains can also be induced by the piezoelectric effect developing when the electric field is applied to the substrate.

The nanodots can be fabricated out of any ferroelectric material, for example, the tensively-strained perovskite oxides, Hf-based oxides, or uniaxial ferroelectrics. Particular attention can be given to the hyperferroelectric materials, LiZnAs, LiBeSb, NaZnSb, LiBeBi [18, 19]. In these materials, the coercive field can achieve values substantially larger than the depolarization electric field, which enables an easy selection of the desired relative strengths of Q_c and Q_s, for example, while temperature and strain are tuning the system. The dielectric spacer can be made out of any high-κ dielectric. The lateral sizes of the nanodots can be scaled down to several nanometers. It is important to prevent the formation of the multidomain structure in the nanodots, the latter must preserve being monodomain nanodots while maintaining carrying the differently-orientated polarizations. To ensure this, the nucleation of the domain wall should require high nucleation energy, which can be achieved, for instance, by increasing the vertical cross-section nanodot area while keeping the lateral nanodot sizes as small as possible. This can be done by elongation of the nanodots along the direction perpendicular to the capacitor plane.

4. The 3-level switching cycles

The three-level logic unit, as mentioned above, comprises two nanodots representing binary units. Accordingly, its energy profile appears as a certain superposition of the energy profiles of these units. The corresponding curves are shown in figure 3; it contains three branches, $W_{+1}(Q)$, $W_0(Q)$, $W_{-1}(Q)$, giving rise to three-branch hysteresis loops of switching between the three branches of the charge-voltage characteristics $V_-(Q) = C_{eff}^{-1}(Q - 2Q_s)$, $V_0(Q) = C_{eff}^{-1}Q$ and $V_+(Q) = C_{eff}^{-1}(Q + 2Q_s)$, corresponding to the logical levels of the 3-level logics, $|-1\rangle$, $|0\rangle$, and $|+1\rangle$. There are three distinct regimes of the topology of the hysteresis loops, determined by the relative strength of the effective charge parameters Q_c and Q_s. The energy profiles of polarization states and transition sequence are exemplified in figure 3(a) for the case $3Q_s > Q_c > 2Q_s$. The terminal points, N_0, correspond to the switching instability of one of the nanodots towards the lowest-energy state with the opposite polarization. The corresponding hysteresis loop with sequential switching between the logical levels $|-1\rangle, |0\rangle$, and $|+1\rangle$ at the critical charges Q_1, Q_2, Q_3, and Q_4 is demonstrated in figure 3(b).

Figures 3(c) and (d) present the energy profile and charge-voltage characteristics realized under the condition $Q_c > 3Q_s$. Although it has three logic levels $|-1\rangle$, $|0\rangle$, and $|+1\rangle$ realized at $Q = 0$, the middle level, $|0\rangle$, is topologically unstable in a sense that once the switching from this logical level to either $|-1\rangle$ or $|+1\rangle$ has occurred, the system can never be switched back to this logical level. Then the two-branches hysteresis loop with switching between $|-1\rangle$ and $|+1\rangle$ logical levels becomes the only effective regime. The switching of the system to this 'hidden' logical level, $|0\rangle$, can be achieved, however, by variation of external parameters, different from the charge, for instance, by thermal cycling, involving passing through the high-temperature
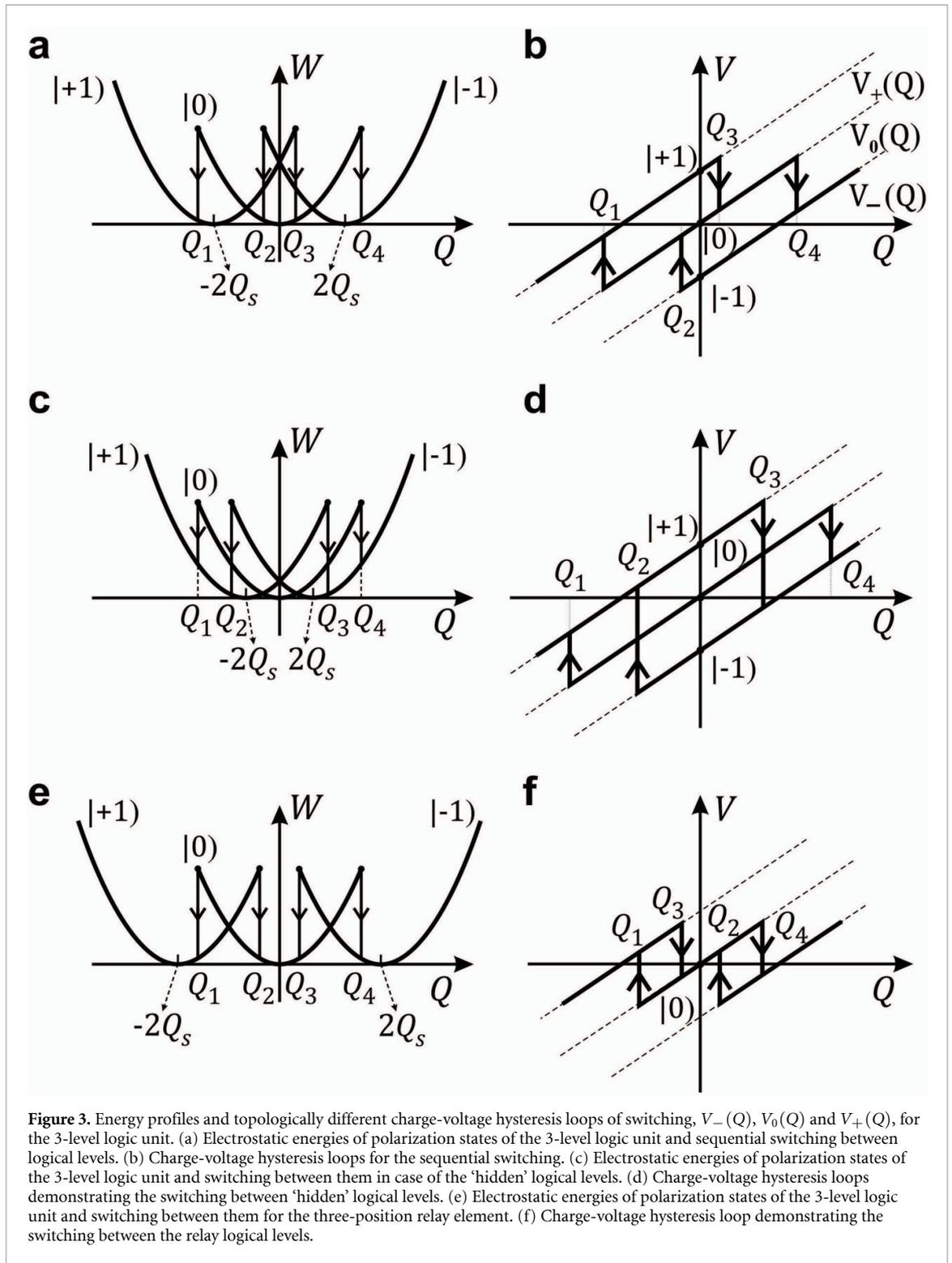
Figure 3. Energy profiles and topologically different charge-voltage hysteresis loops of switching, $V_-(Q)$, $V_0(Q)$ and $V_+(Q)$, for the 3-level logic unit. (a) Electrostatic energies of polarization states of the 3-level logic unit and sequential switching between logical levels. (b) Charge-voltage hysteresis loops for the sequential switching. (c) Electrostatic energies of polarization states of the 3-level logic unit and switching between them in case of the 'hidden' logical levels. (d) Charge-voltage hysteresis loops demonstrating the switching between 'hidden' logical levels. (e) Electrostatic energies of polarization states of the 3-level logic unit and switching between them for the three-position relay element. (f) Charge-voltage hysteresis loop demonstrating the switching between the relay logical levels.

paraelectric state. Figures 3(e) and (f) present the energy profiles and charge-voltage characteristics realized under the condition $Q_c < 2Q_s$. There is only one logic level, $|0\rangle$, at the zero charge, but it presents switching hysteresis zones at finite charges, implementing, thus, the three-position relay element, also known as the Schmitt trigger. Importantly, the hysteresis loops, shown in figure 3 realize all the topologically possible sets of switching in the 3-levels logic [14]. It is the relation between the material-depended critical parameters, Q_s, and Q_c, that determines which topology of the switching is realized. The specific switching protocols can be achieved by the selection of the desired ratio between parameters, Q_s, and Q_c.

Tuning the ratio of the parameters Q_s and Q_c by external stimuli, for example, by temperature and strain, allows for the on-fly modification of the switching logic. This tuning can be done by accounting for different temperature and strain dependencies of these parameters.

Beyond its traditional employment in non-binary circuits as a multi-level memory element, the described multi-level logic units enable a hardware implementation of a neural computing circuit with quantized synaptic weights. An important part of the circuit functioning is the multi-level memristor programming using external fields and temperature pulses. The device can be operated in both the quasi-static tonic regime and the fast spike pulse regime. The necessary dynamic characteristics in the latter regime are regulated by the appropriate resistive element connected in parallel to the logic unit.
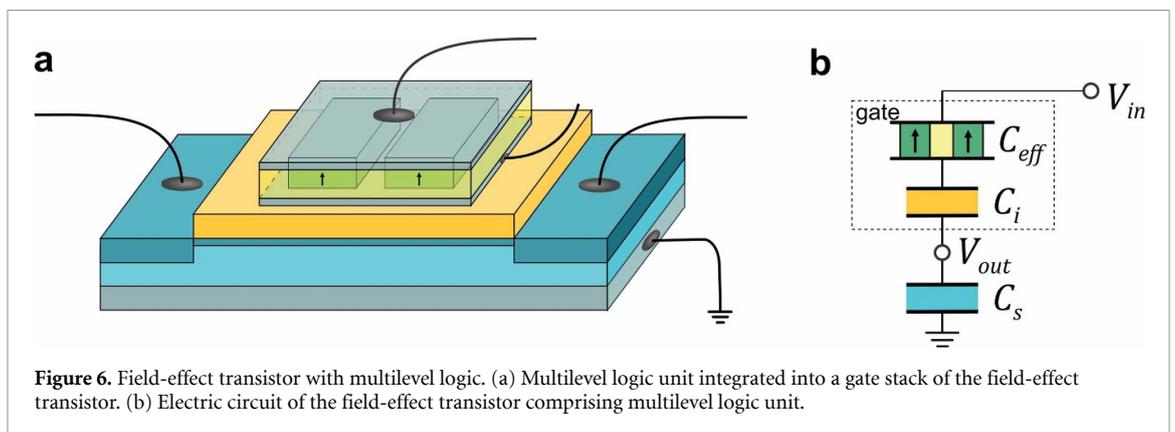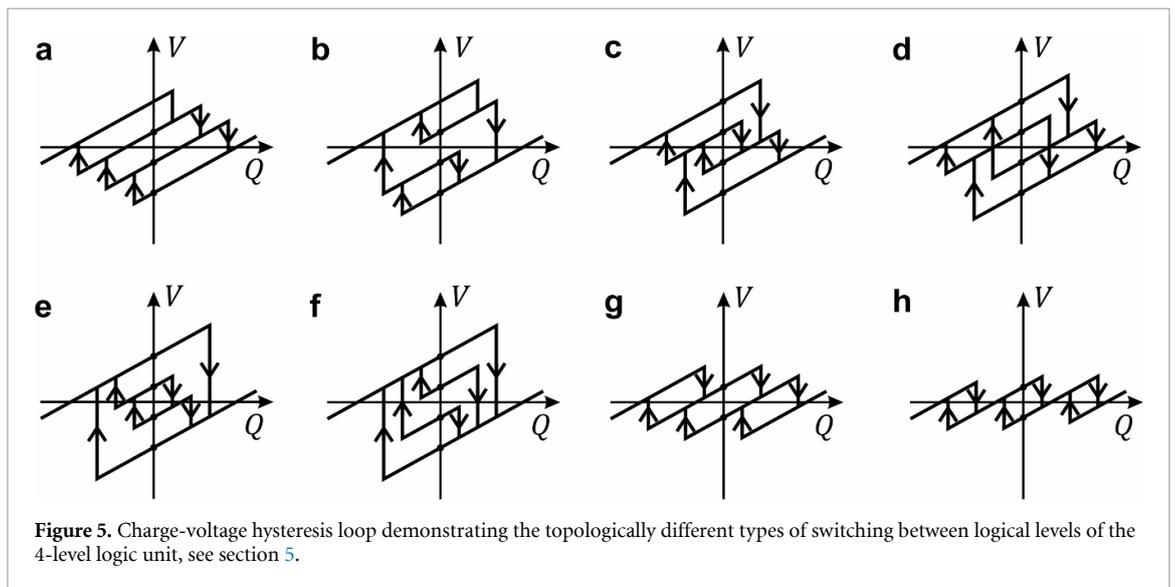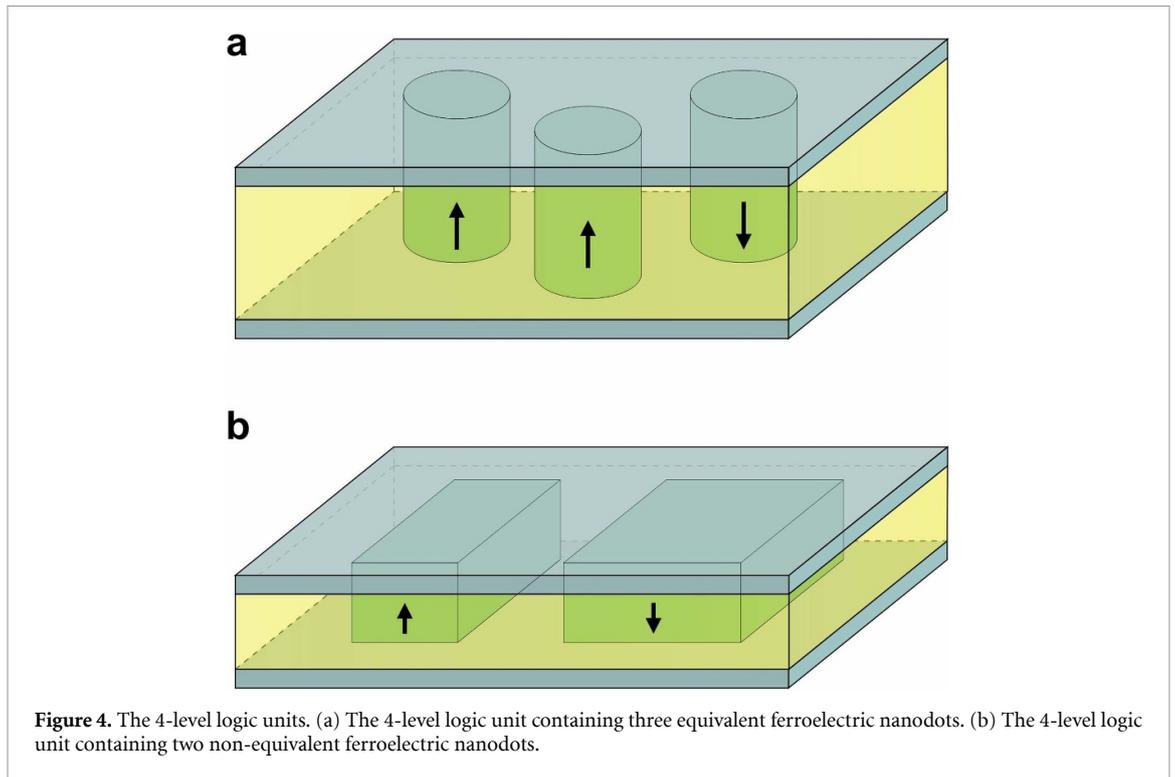
5. The 4-level logic unit and switching cycles

Further enhancement and development bring in logic units implementing the 4-level logic. Figure 4 presents examples of the realization of the topologically configurable 4-level logic units. Figure 4(a) shows an exemplary logic unit in which the three identical, for example, cylindrical ferroelectric nanodots with equal coercive fields and equal cross-sections are confined between the conducting electrodes and are embedded into the dielectric material coating the nanodots and feeling all the remaining free space between conducting electrodes. The state of the system is driven by the electric charge, Q, placed onto conducting plates and providing the set of polarization states, $(+++)$, $(++-)$ (or, equivalently, $(+-+)$ and $(-++)$), $(+--)$, or equivalently, $(-+-)$ and $(--+)$, and, finally, $(---)$. These states realize, thus, the 4-level logic, characterized by the logic levels $|+2\rangle$, $|+1\rangle$, $|-1\rangle$, and $|-2\rangle$, respectively. Figure 4(b) shows another realization of a 4-level logic device. Here two nonequivalent ferroelectric nanodots coated by a dielectric layer are disposed between the conducting electrodes. The nanodots can be made from different ferroelectric materials and may have different sizes. Since the states $(+-)$ and $(-+)$ are now not equivalent, the four polarization states correspond to the logical levels of the 4-level logic unit, namely, $(--) \leftrightarrow |-2\rangle$, $(-+) \leftrightarrow |-1\rangle$, $(+-) \leftrightarrow |+1\rangle$, and $(++) \leftrightarrow |+2\rangle$.

The consideration similar to that given above for the 3-level logic units shows that the hysteresis loops $V(Q)$ for the described 4-level configurations of nanodots have four branches corresponding to the logical levels $|+2\rangle$, $|+1\rangle$, $|-1\rangle$, and $|-2\rangle$. Figure 5 presents all possible typologies of the hysteresis loops with different switching sequences in 4-level logic [14]. The example of the loop with the sequential switching between the levels, driven by changing the charge at the conducting electrodes, is shown in figure 5(a). Figures 5(b)–(h) present other possible examples. The loops in figures 5(a)–(d) correspond to different switching sequences between logical levels that can be used for the design of the four-level logic memories or other processing protocols with different topological ways of accessing the information stored at these levels. The loops in figures 5(e) and (f) correspond to switching loops with the 'hidden' logical levels. Such protocols can be used if the information, stored at the 'hidden levels,' needs to protect from undesirable change and other interferences. Any attempt to access these levels will immediately switch the corresponding information unit to another level with no possibility of the back restoring. Therefore the hysteresis loops provide the security protection of the logic element, which is an especially novel feature of our disclosure. The loops in figures 5(g) and (h) implement the multilevel Schmitt trigger required for multiple applications in electronics. Similar to the case of a 3-level system, the switching sequence (any of the presented in figures 5(a)–(h)) can be selected and modified by the external stimuli, for instance, the temperature or strain, allowing for the on-fly modification of the switching logics.

6. Multilevel field-effect transistor

To implement the control of the circuit currents, the multilevel ferroelectric logic unit can be integrated into a gate stack of the field-effect transistor, see figure 6. Figure 6(a) exemplifies the structure of the corresponding transistor, and figure 6(b) shows the equivalent electric circuit. This device comprises the gate stack overimposed onto a semiconducting substrate (corresponding to the capacitor, C_s, in figure 6(b)) with the grounded bottom electrode in which the source and drain parts are connected by the gate-operated conducting channel. The gate stack includes the ferroelectric multilevel logic unit (corresponding to the capacitor C_{eff} in figure 6(b)) carrying the ferroelectric nanodots coated by the dielectric layer and the gate insulating layer (corresponding to the capacitor C_i in figure 6(b)) separating it from a substrate. This separating layer is a high-κ dielectric layer, preventing the charge leakage between the lower capacitor's electrode and a semiconducting channel. The top electrode of a ferroelectric logic unit is, at the same time, the gate electrode connecting the transistor to an external voltage source, supplying the driving voltage V_{in}. The bottom logic unit electrode is an intermediate electrically isolated floating conducting plate of the transistor that preserves the entire charge (most commonly the zero total charge) constant, stabilizing the logic unit polarization configuration. Furthermore, the floating gate makes the potential along the ferroelectric interface even, maintaining, therefore, a uniform electric field across the gate stack and substrate. The step-wise switching of the voltage, V_{out}, operating the current in the channel under the

Figure 4. The 4-level logic units. (a) The 4-level logic unit containing three equivalent ferroelectric nanodots. (b) The 4-level logic unit containing two non-equivalent ferroelectric nanodots.

Figure 5. Charge-voltage hysteresis loop demonstrating the topologically different types of switching between logical levels of the 4-level logic unit, see section 5.

Figure 6. Field-effect transistor with multilevel logic. (a) Multilevel logic unit integrated into a gate stack of the field-effect transistor. (b) Electric circuit of the field-effect transistor comprising multilevel logic unit.

appropriate protocol for the variation of the driving voltage V_{in} realizes the multilevel logic switching sequence corresponding to one of the topologically possible hysteresis loops, presented above. The logic levels switching order can be modified by external stimuli, for example, by the temperature or strain, allowing for the on-fly modification of the switching logics.

7. Conclusion

The employment of multi-logic devices in neuromorphic computing as multilevel artificial electronic synaptic devices enhances the performance, overcoming the restrictions of binary computing circuits. We have demonstrated that the multilevel logic device can be realized using the ferroelectric unit comprising multiple nanodots disposed between two electrodes. The switching between different polarization configurations of the nanodots is achieved by putting the charge on the electrodes, similar to what happens in the synaptic elements of the brain-inspired logic devices. Importantly, the types of the topology of the multi-level switching can be realized and tuned via external stimuli, temperature, and strain. The suggested ferroelectric logic unit can be integrated into the gate stuck of the field-effect transistor, providing multi-logic control of the current through the transistor channel. We anticipate that harnessing the multi-states features of the suggested device with the negative capacitance effect, emerging in the ferroelectric capacitor with similar charge-controlled architecture [20, 21], will significantly reduce energy consumption for multivalue logic operations. Another opportunity holding high promise is the realization of the artificial neuron with multilevel synaptic weights exploiting the nanoscale multi-state topological formations, domain walls [22], vortices [23], skyrmions [24], and Hopfions [25] integrated into the charge-controlled the confined nanodots due to specific electrostatic interaction in a ferroelectric.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

Acknowledgments

Conflict of interest

The authors declare no competing, financial, or commercial interests in this research.

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